WHAT IS CLAIMED IS:

Claim 1: A liquid crystal display panel comprising:

a display unit comprising pixel elements arranged in a matrix;

a scanning circuit and a signal circuit arranged to drive pixel elements;

a multi-input type level conversion circuit arranged to generate control signals, and to perform level conversion of image signals having a low voltage amplitude into image signals having a high voltage amplitude to the scanning circuit and the signal circuit to drive the pixel elements;

a differential input type level conversion circuit arranged to perform level conversion of differential clock signals having a low voltage amplitude into clock signals having a high voltage amplitude to control transmission of image signal to the signal circuit to drive the pixel elements; and

a latch circuit arranged to latch the image signals having the high voltage amplitude to the signal circuit in accordance with the clock signals having the high voltage amplitude;

wherein the signal circuit and the scanning circuit are driven to provide a visual display of images corresponding to the image signals latched from the latch circuit in accordance with the control signals generated from the multi-input type level conversion circuit.

Claim 2: A liquid crystal display apparatus according to claim 1, wherein the differential input type level conversion circuit comprises:

a first transistor and a second transistor connected in parallel, having respective gate electrodes coupled to receive a bias voltage; and

a first resistance element and a second resistance element connected in parallel, and disposed between respective drain electrodes of the first transistor and the second transistor and a power supply terminal;

wherein respective source electrodes of the first transistor and the second transistor are coupled to receive clock signals having a mutually different polarity and a low voltage amplitude, and the respective drain electrodes of the first transistor and the second transistor are coupled to output clock signals having a mutually different polarity and a high voltage amplitude.

Claim 3: A liquid crystal display apparatus according to claim 2, wherein the differential input type level conversion circuit further includes a waveform shaping unit for shaping a waveform of clock signals having the high voltage amplitude, and comprising:

a third transistor and a fourth transistor connected in parallel, having respective gate electrodes connected to respective drain electrodes of the first transistor and the second transistor, and

a fifth transistor and a sixth transistor connected in parallel, having respective drain electrodes connected to respective drain electrodes of the third transistor and the fourth transistor, and having respective source electrodes connected to a ground terminal,

wherein respective source electrodes of the third transistor and the fourth

transistor are coupled to a power supply terminal, and respective gate electrodes of the fifth transistor and the sixth transistor are connected to respective drain electrodes of the sixth transistor and the fifth transistor.

Claim 4: A liquid crystal display apparatus according to claim 3, wherein the bias voltage is equal to a sum of a peak voltage of clock signals having the low voltage amplitude and a threshold voltage of the first transistor and the second transistor.

Claim 5: A liquid crystal display apparatus according to claim 1, wherein the differential input type level conversion circuit comprises:

a plurality of transistors each having a gate electrode coupled to receive a bias voltage; and

a plurality of resistance elements each connected between a drain electrode of a respective transistor and a power supply terminal;

wherein each of the control signals is inputted to a source electrode of a respective transistor;

wherein each of the control signals is outputted from the drain electrode of a respective transistor; and

wherein amplitudes of the output control signals are higher than amplitudes of the input control signals.

Claim 6: A liquid crystal display apparatus according to claim 5,

wherein each resistance element is comprised of a transistor having a gate electrode biased to a bias voltage.

Claim 7: A liquid crystal display apparatus according to claim 6, wherein the bias voltage is equal to a sum of a peak voltage of the input control signals and a threshold voltage of the transistors.